

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

AMENDMENT(S) TO THE CLAIMS

1
2
3 1. (currently amended): An integrated circuit, comprising:
4 one or more components that receive a distributed voltage; and
5 a voltage driver that produces a compensated voltage;
6 wherein the compensated voltage ~~being is~~ distributed to form the
7 distributed voltage at the one or more components, ~~wherein and~~ the distributed
8 voltage is degraded relative to the compensated voltage; and
9 wherein the voltage driver is responsive to feedback derived from the
10 distributed voltage to adjust the compensated voltage so that the distributed
11 voltage is approximately equal to a nominal voltage.

12
13 2. (original): An integrated circuit as recited in claim 1, wherein said
14 one or more components have input characteristics that contribute to the
15 degradation of the distributed voltage.

16
17 3. (original): An integrated circuit as recited in claim 1, wherein said
18 distribution contributes to the degradation of the distributed voltage.

19
20 4. (original): An integrated circuit as recited in claim 1, wherein:
21 said distribution contributes to the degradation of the distributed voltage;
22 and
23 the compensated voltage is distributed over impedance-matched conductors
24 to form the distributed voltage at the one or more components.
25

1
2 9. (original): An integrated circuit as recited in claim 1, further
3 comprising:

4 a feedback component that evaluates the distributed voltage relative to the
5 nominal voltage to derive said feedback;

6 wherein the voltage driver has a variable gain that is configured to increase
7 in response to the feedback when the distributed voltage is less than the nominal
8 voltage and to decrease in response to the feedback when the distributed voltage is
9 greater than the nominal voltage.

10
11 10. (original): An integrated circuit as recited in claim 1, wherein the
12 voltage driver has a variable gain that is controlled by a digital value.

13
14 11. (original): An integrated circuit as recited in claim 1, wherein the
15 voltage driver has a variable gain that is controlled by a digital value, the
16 integrated circuit further comprising a register that is configurable to store the
17 digital value and to provide the digital value to the voltage driver.

18
19 12. (original): An integrated circuit as recited in claim 1, wherein the
20 voltage driver has a variable gain that is controlled by a digital value, the
21 integrated circuit further comprising a register that is configurable to store the
22 digital value and to provide the digital value to the voltage driver, the register
23 being readable and writable.
24
25

1 13. (original): An integrated circuit as recited in claim 1, wherein the
2 voltage driver has a variable gain that is controlled by a digital value, further
3 comprising a counter that produces the digital value, wherein the counter is
4 responsive to the feedback to increment and decrement the digital value.

5
6 14. (currently amended): An integrated circuit as recited in claim 1,
7 wherein the voltage driver has a variable gain that is controlled by a digital value,
8 further comprising a counter that produces the digital value, wherein the counter is
9 responsive to the feedback during an initialization period to increment and
10 decrement the digital value, and the digital value ~~remaining~~ remains constant
11 during an operational period following the initialization period.

12
13 15. (original): An integrated circuit as recited in claim 1, wherein the
14 integrated circuit comprises a memory device.

15
16 16. (original): An integrated circuit as recited in claim 1, wherein the
17 integrated circuit is a memory device that further comprises a plurality of memory
18 storage cells.

19
20 17. (currently amended): An integrated circuit, comprising:
21 a one or more data receivers that evaluate one or more corresponding data
22 signals relative to a distributed reference voltage; and
23 a reference voltage driver that produces a compensated reference voltage;
24
25

1 wherein the compensated reference voltage ~~being is~~ distributed to form the
2 distributed reference voltage, ~~wherein and~~ the distributed reference voltage is
3 degraded relative to the compensated reference voltage; and

4 wherein the reference voltage driver has a variable gain that increases when
5 the distributed reference voltage is less than a nominal reference voltage and
6 decreases when the distributed reference voltage is greater than the nominal
7 reference voltage.

8
9 18. (original): An integrated circuit as recited in claim 17, wherein the
10 reference voltage driver is configured so that its gain is set during an initialization
11 period and remains constant during a subsequent operational period.

12
13 19. (original): An integrated circuit as recited in claim 17, wherein the
14 variable gain is controlled by a digital value.

15
16 20. (currently amended): An integrated circuit as recited in claim ~~17~~,
17 wherein the variable gain is controlled by a digital value, and the integrated circuit
18 ~~further comprising comprises~~ a register that is configurable to store the digital
19 value and to provide the digital value to the reference voltage driver.

1 21. (currently amended): An integrated circuit as recited in claim ~~17~~,
2 wherein the variable gain is controlled by a digital value, and the integrated circuit
3 ~~further comprising~~ comprises a register that is configurable to store the digital
4 value and to provide the digital value to the reference voltage driver; and wherein
5 the register ~~being~~ is readable and writable.

6
7 22. (original): An integrated circuit as recited in claim 17, wherein the
8 variable gain is controlled by a digital value, further comprising a counter that
9 produces the digital value, wherein the counter increments or decrements the
10 digital value depending on the relationship of the distributed reference voltage
11 relative to the nominal reference voltage.

12
13 23. (currently amended): An integrated circuit as recited in claim 17,
14 wherein the variable gain is controlled by a digital value, and the integrated circuit
15 further comprises a counter that produces the digital value; wherein the counter is
16 configured to increase and decrease the digital value during an initialization period
17 depending on the relationship of the distributed reference voltage and the nominal
18 reference voltage, and the digital value ~~remaining~~ remains constant during an
19 operational period following the initialization period.

20
21 24. (original): An integrated circuit as recited in claim 17, further
22 comprising a capacitive charge pump that controls the gain of the reference
23 voltage driver.

1 25. (currently amended): An integrated circuit as recited in claim 17,
2 further comprising a feedback component that evaluates the distributed reference
3 voltage relative to the nominal reference voltage to generate a feedback signal,
4 wherein the reference voltage driver-being-response is responsive to the feedback
5 signal to increase and decrease the variable gain.

6
7 26. (currently amended): An integrated circuit as recited in claim 17,
8 further comprising:

9 a feedback component that evaluates the distributed reference voltage
10 relative to the nominal reference voltage to generate a feedback signal;

11 a charge pump that produces a control voltage to establish the gain of the
12 reference voltage driver;

13 wherein the charge pump-being is responsive to the feedback signal to
14 increase and decrease the variable gain.

15
16 27. (original): An integrated circuit as recited in claim 17, wherein the
17 compensated reference voltage is distributed over impedance-matched conductors
18 to form the distributed reference voltage at the one or more data receivers.

19
20 28. (currently amended): An integrated circuit as recited in claim 17,
21 further comprising:

22 a feedback component that evaluates the distributed reference voltage
23 relative to the nominal reference voltage to generate a feedback signal, wherein
24 the reference voltage driver-being-response is responsive to the feedback signal to
25 increase and decrease the variable gain;

1 wherein the feedback component incorporates a low-pass filter.

2
3 29. (original): An integrated circuit as recited in claim 17, wherein the
4 one or more data receivers comprise a plurality of the data receivers, and wherein
5 the data receivers have similar input characteristics and the distributed reference
6 voltage is routed similarly to each of the data receivers to result in similar
7 degradation of the distributed reference voltage at each of the data receivers.

8
9 30. (currently amended): An integrated circuit as recited in claim 17,
10 further comprising:

11 a feedback receiver that evaluates the distributed reference voltage relative
12 to the nominal reference voltage to generate a feedback signal, wherein the
13 reference voltage driver ~~being response~~ is responsive to the feedback signal to
14 increase and decrease the variable gain;

15 wherein the data and feedback receivers have similar input characteristics
16 and the distributed reference voltage is routed similarly to the data and feedback
17 receivers to result in similar degradation of the distributed reference voltage at the
18 data and feedback receivers.

19
20 31. (currently amended): An integrated circuit as recited in claim 17,
21 further comprising:

22 a feedback receiver that evaluates the distributed reference voltage relative
23 to the nominal reference voltage to generate a feedback signal, wherein the
24 reference voltage driver ~~being response~~ is responsive to the feedback signal to
25 increase and decrease the variable gain;

1 wherein the data and feedback receivers have similar input characteristics
2 and the distributed reference voltage is routed similarly to the data and feedback
3 receivers to result in similar degradation of the distributed reference voltage at the
4 data and feedback receivers; and

5 wherein the feedback receiver incorporates a low-pass filter that does not
6 significantly affect the input characteristics of the feedback receiver.

7
8 32. (original): An integrated circuit as recited in claim 17, wherein the
9 integrated circuit is a memory device that further comprises a plurality of memory
10 storage cells.

11
12 33. (currently amended): An integrated circuit, comprising:
13 a plurality of data receivers that evaluate corresponding data signals relative
14 to a distributed reference voltage;

15 a feedback receiver that evaluates the distributed reference voltage relative
16 to a nominal reference voltage to produce a feedback signal;

17 a reference voltage driver that produces a compensated reference voltage;

18 wherein the compensated reference voltage ~~being~~ is routed on the
19 integrated circuit to form the distributed reference voltage at the data and feedback
20 receivers, ~~wherein~~ and the input characteristics of the data and feedback receivers
21 cause a voltage change in the distributed reference voltage at each receiver relative
22 to the compensated reference voltage;

23 wherein the data and feedback receivers ~~having~~ have similar input
24 characteristics so that said relative voltage change in the distributed reference
25 voltage is approximately the same at each of the data and feedback receivers;

1 an increment/decrement component that produces a digital value in
2 response to the feedback signal, wherein the increment/decrement component
3 being is configured to increment and decrement the digital value depending on the
4 relationship of the distributed reference voltage and the nominal reference voltage
5 as indicated by the feedback signal; and

6 wherein the reference voltage driver has a variable gain that is established
7 by the digital value.

8
9 34. (original): An integrated circuit as recited in claim 33, wherein the
10 compensated reference voltage is distributed over impedance-matched conductors
11 to form the distributed reference voltage at the data and feedback receivers.

12
13 35. (original): An integrated circuit as recited in claim 33, wherein the
14 increment/decrement component is enabled during an initialization period and the
15 digital value remains constant during a subsequent operational period.

16
17 36. (original): An integrated circuit as recited in claim 33, further
18 comprising a register that is configurable to store the digital value and to provide
19 the digital value to the reference voltage driver.

20
21 37. (currently amended): An integrated circuit as recited in claim 33,
22 further comprising a register that is configurable to store the digital value and to
23 provide the digital value to the reference voltage driver, wherein the register-being
24 is readable and writable.
25

1 38. (original): An integrated circuit as recited in claim 33, further
2 comprising a digitally controllable variable resistor that controls the gain of the
3 reference voltage driver.

4
5 39. (original): An integrated circuit as recited in claim 33, wherein the
6 feedback receiver comprises a low-pass filter that does not significantly affect the
7 input characteristics of the feedback receiver.

8
9 40. (original): An integrated circuit as recited in claim 33, wherein the
10 distributed reference voltage is routed similarly to the data and feedback receivers
11 so that said relative voltage change in the distributed reference voltage is
12 approximately the same at each of the data and feedback receivers.

13
14 41. (original): An integrated circuit as recited in claim 33, wherein:
15 the distributed reference voltage is routed similarly to the data and feedback
16 receivers so that said relative voltage change in the distributed reference voltage is
17 approximately the same at each of the data and feedback receivers; and
18 the feedback receiver comprises a low-pass filter that does not significantly
19 affect the input characteristics of the feedback receiver.

20
21 42. (original): An integrated circuit as recited in claim 33, wherein the
22 integrated circuit is a memory device that further comprises a plurality of memory
23 storage cells.
24
25

1 43. (currently amended): An integrated circuit, comprising:
2 receiver means for evaluating a plurality of data signals relative to a
3 distributed reference voltage;
4 feedback means for evaluating the distributed reference voltage relative to a
5 nominal reference voltage to produce a feedback signal;
6 driver means having a variable gain for producing a compensated reference
7 voltage;
8 routing means for routing the compensated reference voltage on the
9 integrated circuit to form the distributed reference voltage at the receiver and
10 feedback means;
11 wherein the input characteristics of the receiver and feedback means cause
12 a voltage change in the distributed reference voltage at the receiver and feedback
13 means relative to the compensated reference voltage;
14 wherein the receiver and feedback means~~having~~ have similar input
15 characteristics so that said relative voltage change in the distributed reference
16 voltage is approximately the same at each of the receiver and feedback means; and
17 gain control means for controlling the gain of the driver means in response
18 to the feedback signal so that the distributed reference voltage is approximately
19 equal to the nominal reference voltage.

20
21 44. (original): An integrated circuit as recited in claim 43, wherein the
22 gain control means comprises a counter that produces a digital value, wherein the
23 counter is responsive to the feedback to increment and decrement the digital value.
24
25

1 45. (currently amended): An integrated circuit as recited in claim 43,
2 wherein the gain control means comprises a register that is configurable to store a
3 digital value, and wherein the variable gain of the driver means-being is responsive
4 to the digital value.

5
6 46. (currently amended): An integrated circuit as recited in claim 43,
7 wherein the gain control means comprises a register that is configurable to store a
8 digital value, the variable gain of the driver means-being is responsive to the
9 digital value, and the register-being is readable and writable.

10
11 47. (original): An integrated circuit as recited in claim 43, wherein the
12 compensated reference voltage is distributed over impedance-matched conductors
13 to form the distributed reference voltage at the receiver and feedback means.

14
15 48. (original): An integrated circuit as recited in claim 43, wherein the
16 gain control means is enabled during an initialization period to adjust the gain of
17 the driver means, wherein the gain control means is configured to maintain the
18 gain of the driver means constant during a subsequent operational period.

19
20 49. (original): An integrated circuit as recited in claim 43, wherein the
21 gain control means comprises a digitally controllable variable resistor.
22
23
24
25

1 50. (original): An integrated circuit as recited in claim 43, wherein the
2 distributed reference voltage is routed similarly to the receiver and feedback
3 means so that said relative voltage change in the distributed reference voltage is
4 approximately the same at each of the receiver and feedback means.

5
6 51. (currently amended): An integrated circuit as recited in claim 43,
7 wherein:

8 ~~wherein~~ the distributed reference voltage is routed similarly to the receiver
9 and feedback means so that said relative voltage change in the distributed
10 reference voltage is approximately the same at each of the receiver and feedback
11 means; and

12 the feedback means comprises a low-pass filter that does not significantly
13 affect the input characteristics of the op-amp.

14
15 52. (original): An integrated circuit as recited in claim 43, wherein the
16 integrated circuit is a memory device that further comprises a plurality of memory
17 storage cells.

18
19 53. (currently amended): A memory device comprising:
20 a plurality of memory storage cells;
21 a plurality of data receivers that evaluate binary data signals with reference
22 to a distributed reference voltage;
23 a feedback receiver that evaluates the distributed reference voltage relative
24 to a nominal reference voltage to produce a feedback signal;
25 a reference voltage driver that produces a compensated reference voltage;

1 wherein the compensated reference voltage ~~being~~ is routed on the memory
2 device to form the distributed reference voltage at the data and feedback receivers,
3 wherein and the input characteristics of the data and feedback receivers cause a
4 voltage change in the distributed reference voltage at each receiver relative to the
5 compensated reference voltage;

6 wherein the data and feedback receivers ~~having~~ have similar input
7 characteristics so that said relative voltage change in the distributed reference
8 voltage is approximately the same at each of the data and feedback receivers; and

9 wherein the reference voltage driver has a variable gain that is configurable
10 to increase in response to the feedback signal when the distributed reference
11 voltage is less than the nominal reference voltage and to decrease in response to
12 the feedback signal when the distributed reference voltage is greater than the
13 nominal reference voltage.

14
15 54. (original): A memory device as recited in claim 53, wherein the
16 compensated reference voltage is distributed over impedance-matched conductors
17 to form the distributed reference voltage at the data and feedback receivers.

18
19 55. (original): A memory device as recited in claim 53, wherein the
20 variable gain of the reference voltage driver is controlled by a digital value, the
21 integrated circuit further comprising a register that is configurable to store the
22 digital value and to provide the digital value to the reference voltage driver.

1 56. (currently amended): A memory device as recited in claim 53,
2 wherein the variable gain of the reference voltage driver is controlled by a digital
3 value, and the integrated circuit further comprising comprises a register that is
4 configurable to store the digital value and to provide the digital value to the
5 reference voltage driver; and wherein the register being is readable and writable.
6

7 57. (original): A memory device as recited in claim 53, wherein the gain
8 of the reference voltage driver remains constant during an operational period that
9 follows an initialization period.
10

11 58. (original): A memory device as recited in claim 53, wherein the
12 feedback receiver comprises a low-pass filter that does not significantly affect the
13 input characteristics of the feedback receiver.
14

15 59. (original): A memory device as recited in claim 53, wherein:
16 the distributed reference voltage is routed similarly to the data and feedback
17 receivers so that said relative voltage change in the distributed reference voltage is
18 approximately the same at each of the data and feedback receivers; and
19 the feedback receiver comprises a low-pass filter that does not significantly
20 affect the input characteristics of the feedback receiver.
21

22 60. (currently amended): A method comprising:
23 evaluating a plurality of signals relative to a distributed voltage;
24 amplifying a nominal voltage by a variable gain to produce a compensated
25 reference voltage;

1 routing the compensated reference voltage over resistive conductors to form
2 the distributed voltage;

3 increasing the variable gain when the distributed voltage is less than the
4 nominal voltage; and

5 decreasing the variable gain when the distributed voltage is greater than the
6 nominal voltage.

7
8 61. (original): A method as recited in claim 60, wherein the routing
9 comprises routing the compensated reference voltage over impedance-matched
10 resistive conductors to form the distributed voltage.

11
12 62. (original): A method as recited in claim 60, further comprising:
13 maintaining the variable gain at a constant value during an operational
14 period following an initialization period.

15
16 63. (new): An integrated circuit, comprising:
17 a reference voltage driver that has a variable gain and produces a
18 compensated reference voltage; and

19 a plurality of receivers that evaluate signals relative to a distributed
20 reference voltage, a particular receiver of the plurality of receivers capable of
21 evaluating a nominal reference voltage signal relative to the distributed reference
22 voltage to produce a feedback signal;

23 wherein the compensated reference voltage is distributed to form the
24 distributed reference voltage, and the distributed reference voltage is degraded
25 relative to the compensated reference voltage; and

1 wherein the reference voltage driver is responsive to the feedback signal
2 such that the variable gain increases when the distributed reference voltage is less
3 than the nominal reference voltage signal and decreases when the distributed
4 reference voltage is greater than the nominal reference voltage signal.

5
6 64. (new): An integrated circuit as recited in claim 63, wherein the
7 particular receiver is useable during an initialization period to evaluate the
8 nominal reference voltage signal relative to the distributed reference voltage to
9 produce the feedback signal and is unused during an operational period.

10
11 65. (new): An integrated circuit as recited in claim 63, wherein the
12 particular receiver is useable during an initialization period to evaluate the
13 nominal reference voltage signal relative to the distributed reference voltage to
14 produce the feedback signal and is useable during an operational period to
15 evaluate a data signal relative to the distributed reference voltage.

16
17 66. (new): An integrated circuit as recited in claim 63, wherein the
18 compensated reference voltage is distributed over impedance-matched conductors
19 to form the distributed reference voltage at the plurality of receivers.
20
21
22
23
24
25

1 67. (new): An integrated circuit as recited in claim 63, wherein the
2 plurality of receivers have input characteristics that cause a voltage change in the
3 distributed reference voltage at each receiver relative to the compensated reference
4 voltage; and wherein the input characteristics are similar such that the relative
5 voltage change in the distributed reference voltage is approximately the same at
6 each receiver of the plurality of receivers.

7
8 68. (new): An integrated circuit as recited in claim 63, wherein the
9 particular receiver includes a low-pass filter that does not significantly affect input
10 characteristics of the particular receiver.

11
12 69. (new): An integrated circuit as recited in claim 63, further
13 comprising memory storage cells.

14
15 70. (new): An integrated circuit as recited in claim 63, wherein the
16 variable gain of the reference voltage driver is controlled by a digital value.

17
18 71. (new): An integrated circuit as recited in claim 63, further
19 comprising a register that is configurable to store a digital value; wherein the
20 variable gain of the reference voltage driver is controllable by the digital value of
21 the register.

1 72 (new): An integrated circuit as recited in claim 63, wherein the
2 reference voltage driver includes a counter that can change the variable gain of the
3 reference voltage driver responsive to the feedback signal.
4

5 73 (new): An integrated circuit as recited in claim 63, further
6 comprising a charge pump that produces a control voltage to establish the variable
7 gain of the reference voltage driver; wherein the charge pump is responsive to the
8 feedback signal to cause the variable gain to increase or decrease.
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25